DC FEE Review

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Organization and Management

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Kim Minuzzo, DC FEE Lead Engineer (LLNL)

Chuck Pancake, DC FEE Engineer (Stonybrook)

Leonid Kudin, DC HV Engineer (PNPI)

Daryl Autrey, DC FEE Implementer (LLNL)

Bob Petersen, DC FEE Lead Engineer Alumnus (LLNL)

- LLNL will complete the design and prototype production of the ASDTMC and the FEM boards.
- LLNL and Stonybrook will jointly test the prototype boards and coordinate the final design.
- Stonybrook will coordinate final board production, testing, validation and installation; LLNL will act only in an advisory role during board production and testing.

DC FEE Components

- Chamber frame and sense wires (PNPI)
- 80 HV. Board -> absolute signal ground, mechanical foundation for the FEEs.
    - Signal interface -> solder/mechanical connections + mounting connectors (24-pin Futurebus+)
- 320 ASDTMC boards - 40 ch/brd * 4 brds/keystone * 80 keystone =12,800 channels
    - ASD8 circuit -> preamp, shaper, discriminator package from UPenn
    - TMC circuit -> pipeline TDC with 5-event buffer & output FIFO from KEK
- 80 FEM control boards -> top board containing ArcNET/GLink/FPGA controls
    - ArcNET circuit/interface (PHENIX/BNL)
    - GLink interface (BNL)
    - Heap Manager - Altera FPGA to be designed by Stonybrook assisted by LLNL
- Power distribution/isolation (BNL)
- Shielding and Ground management (LLNL/StonyBrook)

Specifications: HV board and signal input

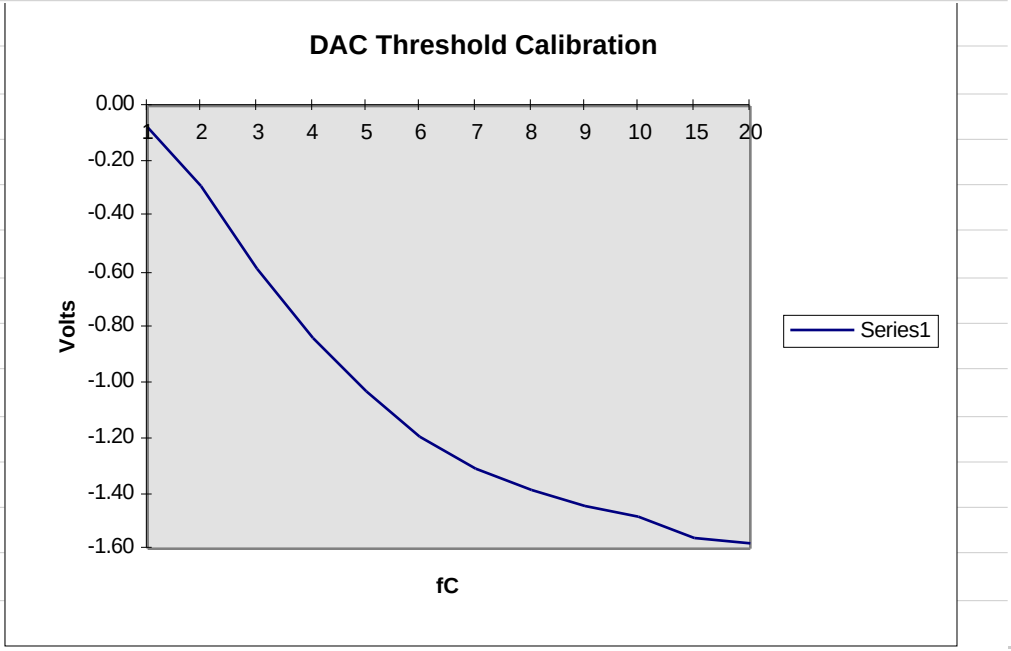
- HV board size determined by chamber frame specifications.
- HV connector currently AMP 9-position MATE-N-LOK, LGH for RG59 coax.
- ASDTMC board connectors are 24-pin Futurebus+; locations have been fixed to minimize input signal trace length.
- Connections from wires to ASDTMC boards are still unspecified -> need to specify flex versus ribbon cables and connection from feedthru cable to HV board.
- Signal ground issues on HV board are understood and will be implemented in next revision of HV board.
- Maximum voltage on HV board is approximately 4500 V.

Specifications for ASDTMC board

- Board size/layout/location determined by chamber frame specifications and optimal use of available space: ASD8 and TMC chips on a single board.
- Signal input: < +/- 3V, < 3-5mA.
- Input protection: Implemented on "-" with diodes, under evaluation on "+" (needed).
- ASD8 to TMC: Differential +/- 150mV @1.8V (TMC input designed for ASD8 output).
- Total number of channels: 12,800 (12,736 active sense wires due to loss of U, V at the arc ends).
- Pulser: Single shot, serially controlled, all channels simultaneously.
- Threshold control: Individual channels, serially controlled, 0 to 15 fC range.
    - Threshold control can be used to turn channel off.

DAC Threshold Calibration

	Threshold	
fC	DAC Value	Volts
1	124	-0.08
2	113	-0.29
3	98	-0.59
4	85	-0.84
5	75	-1.04
6	67	-1.19
7	61	-1.31
8	57	-1.39
9	54	-1.45
10	52	-1.48
15	48	-1.56
20	47	-1.58



Specifications for ASDTMC board: cont.

- x1 Temperature sensor per board
- Individual ASD8 chip power and ground moating.
- On board power regulation.
- Power : 15W
- Thermal conduction to water-cooled chamber frame (Stonybrook)
- Outputs from ASD8 are buried under TMC ground planes on both sides of board.
- RF shielding mid-board between ASD8 and TMC chips

The LLNL prototype ASD8 board has been run on DC test chamber at 2 fC thresholds. The ASDTMC board will be constructed from the proven ASD8 prototype board (design & layout).

ASD8 production specifications

- Proven chip design from UPenn (Mitch Newcomer)
- No. of channels: 8
- Shaping time: 6-ns shaping
- Chip size: 1-cm^2 plastic pack
- Time-over-threshold: approximately 20-ns (satisfies two-track resolution physics specification).
- Schedule

2100 ASD-8 chips ordered	Jul 96
Maxxim production complete	Nov 96
Chips Packaged	Dec 96
Testing at UPenn Begins	Jan 97
Delivery of 1st Lot to PHENIX	Feb 97
Delivery of Tested Chips complete	May 97

PHENIX has considerable experience with the ASD8 chip; considerable literature exists on the ASD8 design and operation. For example, see F. M. Newcomer, S. Tedja, R. Van Berg, J. Van der Spiegel and H. H. Williams, IEEE Trans on Nucl. Sci., **40**, No. 4, 630 (1993).

TMC-PHX production specifications

• Proven chip design by Yasuo Arai at KEK based on TMC1001, TMC1004, TMCTEG3 (packaged as commercially successful VME and CAMAC modules).

• 0.5-micron CMOS Sea-of-Gates technology.

• No. of channels: 4.

• Resolution: 828-ps @4x RHIC.

• Maximum drift time: 530-ns (20 word readout depth is original PHENIX specification; each word is based on a 32-bit PLL with each bit clocked to 828-ps).

• 5-event buffer (6.4 satisfies PHENIX trigger specification).

• On-chip FIFO and logic for untangling overlapping events.

• Leading and Trailing Edge readout: LE possible every 13.25-ns; LE takes priority over trailing edge.

• Asynchronous read and write => no intrinsic dead time.

• Schedule

Design and simulation of TMC-PHX (4channel)	Sep-Oct 96
Layout and Submission of TMC-PHX prototype	Nov 96
Testing of TMC-PHX prototype chip	Jan 97

Specifications for FEM board

- 2 GLink Modules clocked @4x RHIC clock = 714 Mbits/sec each
- 4x RHIC clock on TMC (input and output); 4x RHIC clock on GLink.

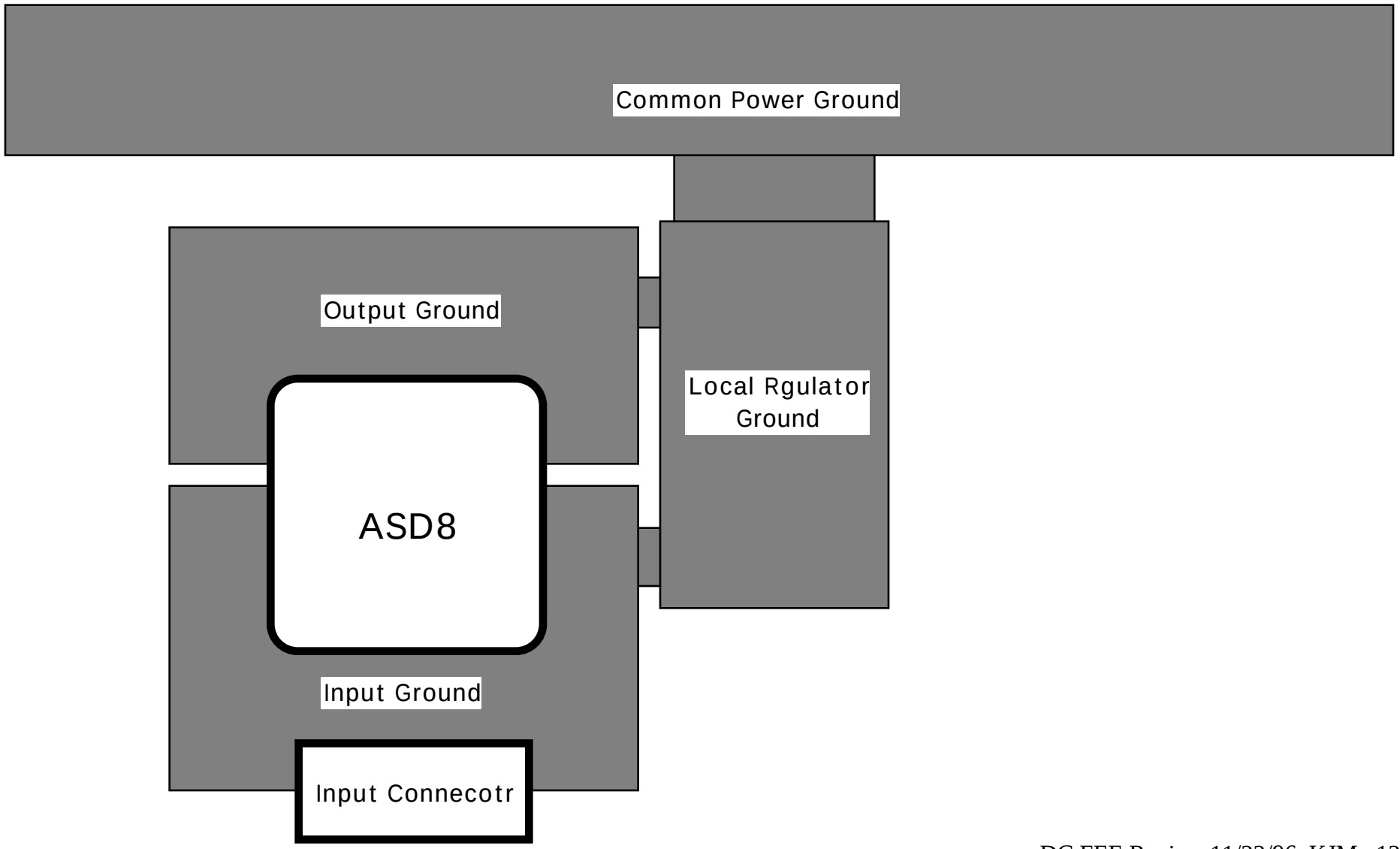
  Readout 20 10-bit words per channel per trigger => 32kbits/trigger

  @4x RHIC => 22.4 usec readout over 2 GLinks
- Heap Manager : Altera FPGA@4x RHIC clock
- Arcnet Module - 5Mbits/sec
- Timing & Control inputs
- Power regulation/distribution to ASDTMC boards.
- Power : 25 Watts

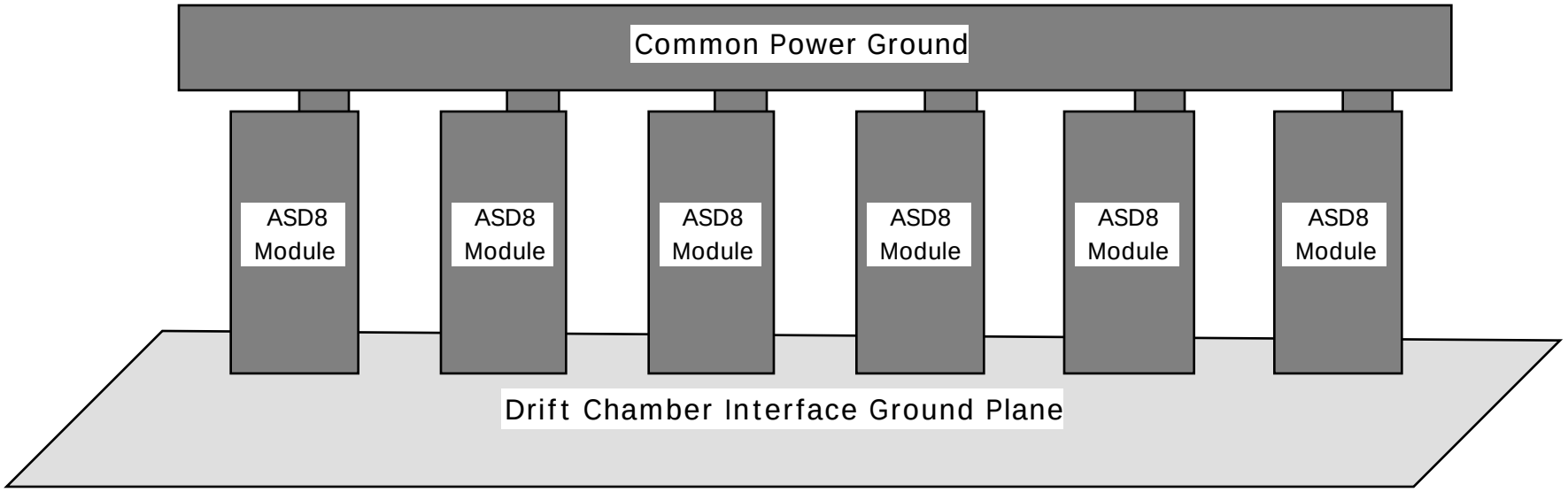
Grounding and Shielding Issues

- Grounding
  - Signal ground is at the DC Interface, i.e. HV board.
    - Must be common ground point
    - Must have very low impedance
      - Contiguous Ground plane
    - Final grounding strategies depend on DC test results at Stonybrook.
- Shielding
  - Ground wings shielding analog/digital sections
    - May also need inter-board shielding
      - (See Stonybrook tests)
  - Final shielding strategies depend on DC test results at Stonybrook.
- In hind sight, it would have been benifical to have Soneybrook immediately pursue a redesign of the DC interface card to make sure we're on the right track with grounding and shielding.

Local Amplifier Ground Detail



ASDTMC / HV Board Ground Interface



LV Power Supply Issues

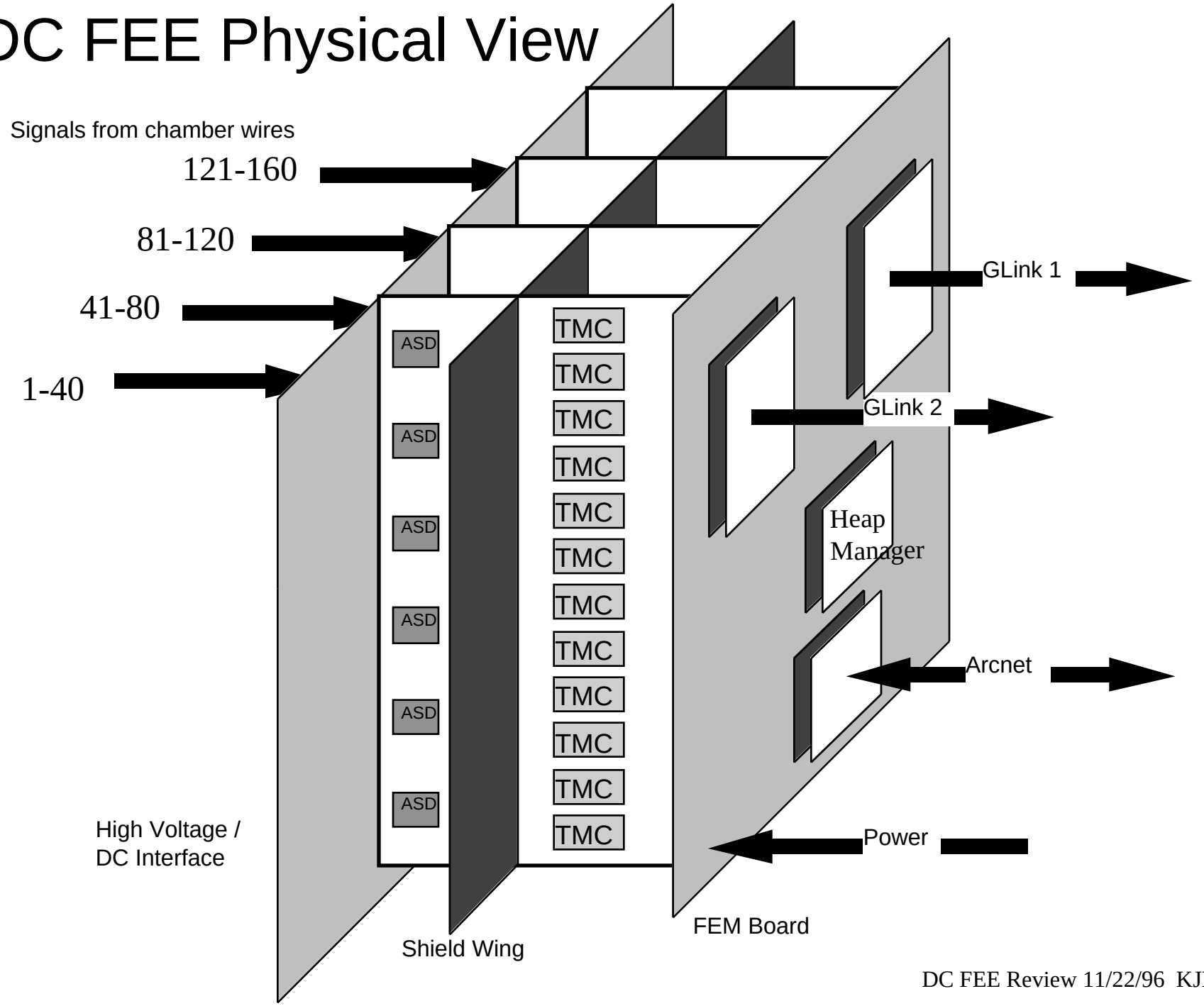
- Must use linear supplies
- Each Keystone should have its own isolated supplies
    - +/- 5 Volts for Analog
    - +/- 5 Volts for Digital
        - -5 V only for Special Arcnet module
- LV power supply lines to Keystone short as possible
    - Long lines produce intolerable IR drops
        - Required cables can be large
    - Long lines require additional regulators on board
        - Can't use 5 volts directly. Must start with 7 - 8 volts and regulate down
        - Already cramped for real estate

Keystone Power Budget

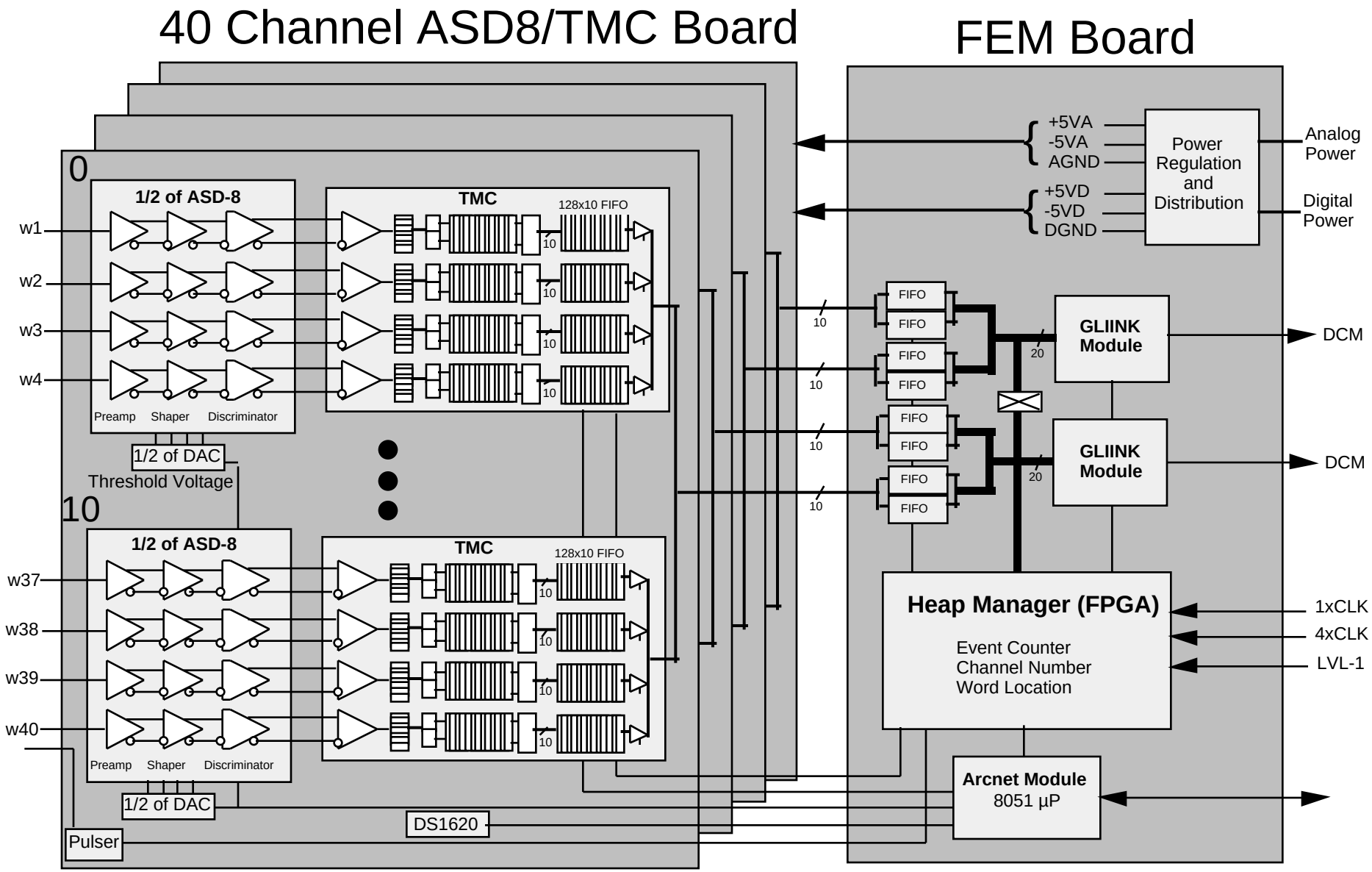
		Regulators									
Component	**+3.3 V**	**+2.5 V**	**+3 V**	**-3 V**	**+5 V**	**-5 V**	**Prts/Brd**	**Brds/Key**	**I/Brd**	**I/Key**	**Power**
Analog											
ASD8		30 mA	50 mA	50 mA			6	4	0.78 A	3.12 A	15.6 W
DAC					25 mA	25 mA	6	4	0.30 A	1.20 A	6.0 W
ASD Test Pulser					120 mA		1	4	0.12 A	0.48 A	2.4 W
									1.20 A	4.80 A	**24.0 W**
Digital											
TMC	*175 mA*						10	4	1.75 A	7.00 A	35.0 W
Buffers					*200 mA*		1	4	0.20 A	0.80 A	4.0 W
Altera	*400 mA*						1	1	0.40 A	0.40 A	2.0 W
GLink					*1000 mA*		2	1	2.00 A	2.00 A	10.0 W
ArcNet					*500 mA*	*100 mA*	1	1	0.60 A	0.60 A	3.0 W
FIFO					*100 mA*		8	1	0.80 A	0.80 A	4.0 W
Buffers					*400 mA*		1	1	0.40 A	0.40 A	2.0 W
Totals										12.00 A	**60.0 W**
		*Italic entries are estimates								**Keystone Total**	**84.0 W**

Approximately 85W/keystone => 6.8kW total for chamber

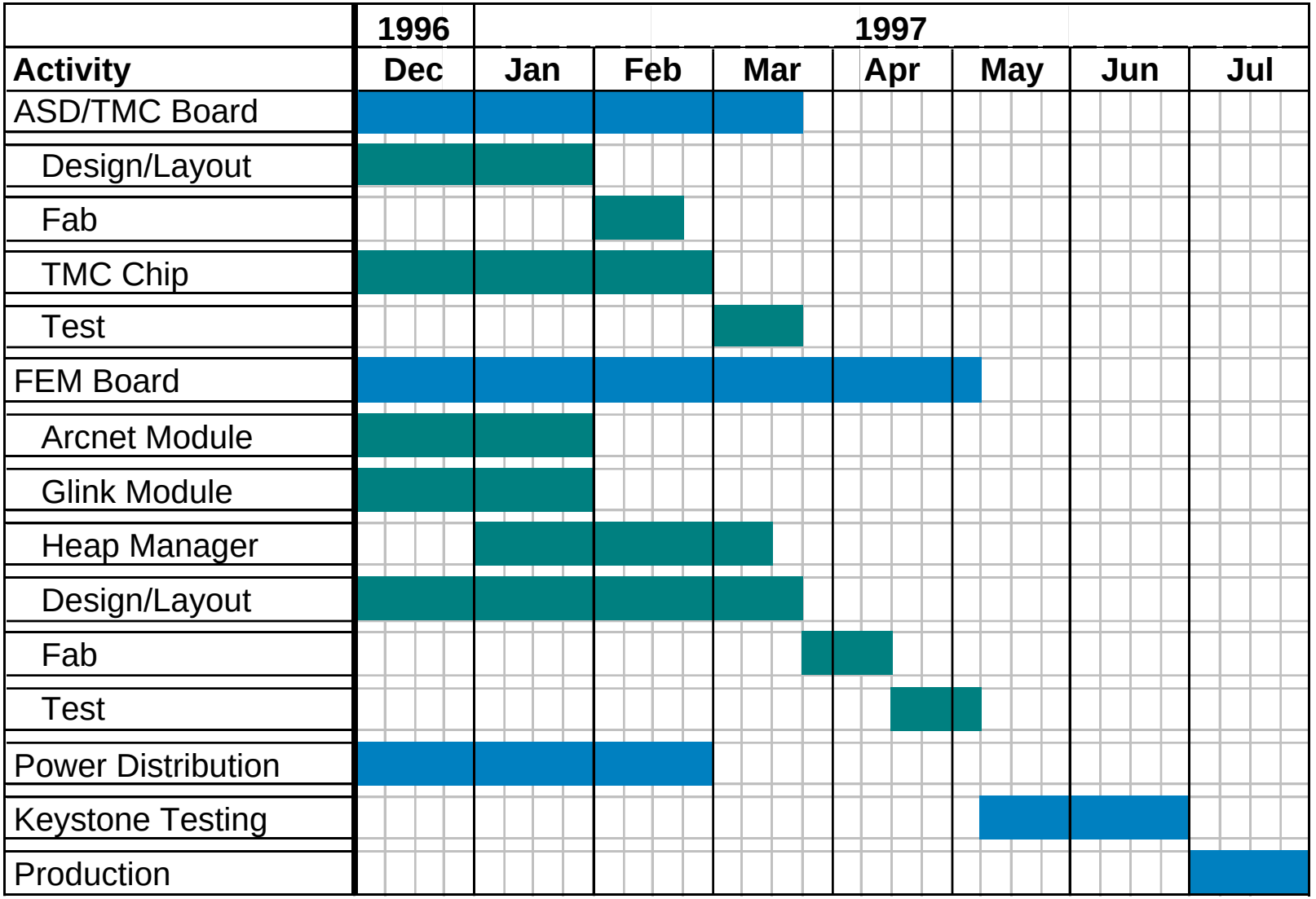
DC FEE Physical View



DC FEE Block Diagram



Schedule


1996
1997
Activity
Dec
Jan
Feb
Mar
Apr
May
Jun
Jul
ASD/TMC Board
Design/Layout
Fab
TMC Chip
Test
FEM Board
Arcnet Module
Glink Module
Heap Manager
Design/Layout
Fab
Test
Power Distribution
Keystone Testing
Production

Issues

- Pulser implementation on input ribbon versus input flex cable.
- Signal input scheme on flex cable from HV board to ASDTMC board
    1. “+” line run next to “-” line for CMR
    2. “+” left floating @ ASD-8 input & gnds run between signal lines
- H.V. Board design and ground -> perhaps the most important issue for FEE.
- External Low Voltage distribution to FEM -> x2 analog, x2 digital (+/- 5 V each).
- GLink daughter card footprint and power consumption.
- ArcNET daughter card footprint and power consumption.
- TMCPHX design/production -> TMC-TEG5 (PHX prototype) did not work...
- DAQ for testing -> DCM-D not ready for 1-yr; however, DCM-T will likely work.